Lasertec

PRESS RELEASE

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Lasertec Releases OLIC Series Die-to-Wafer Overlay Measurement System for Die-to-Wafer Stacking Process

Yokohama, November 27, 2026 – Lasertec Corporation today announced the release of the OLIC Series, a new measurement system designed for the high-speed, high-precision measurement of wafer alignment marks.

The OLIC contributes to higher-quality stacking by enabling fast and precise measurement of wafer alignment marks used to bond chips (dies) diced from wafers onto other wafers during Die-to-Wafer[1] stacking processes.

As advanced packaging technologies continue to evolve, Die-to-Wafer stacking processes are being increasingly adopted across a wide range of semiconductor devices. In Wafer-to-Wafer[2] stacking, relatively large alignment marks can be placed on scribe lines, enabling overlay measurements using transmitted light. In contrast, the Die-to-Wafer method does not provide scribe lines because stacking is performed after dicing. As a result, alignment marks must be placed within the chip area, requiring significantly smaller mark sizes. Furthermore, because active device structures exist beneath the alignment marks, transmitted-light inspection is not feasible, creating a need for highly reproducible inspection using reflected light.

The OLIC utilizes an infrared light source to detect reflected light from alignment marks on wafers while allowing the light to penetrate silicon. Although the use of infrared light generally reduces image resolution and contrast, Lasertec's uniquely designed optics technology enables the system to capture high-resolution, high-contrast images at high throughput, even for extremely small alignment marks. Through this technology, the OLIC helps optimize process control and improve stacking accuracy in Die-to-Wafer stacking processes.

Lasertec remains committed to delivering innovative inspection solutions for leading-edge semiconductor packaging that enhance the quality and productivity of semiconductor manufacturing processes

1 Die-to-Wafer: Stacking method to bond chip (die) cut from a wafer onto a separate wafer.
2 Wafer-to-Wafer: Stacking method to bond wafers.

Features

- Measures alignment marks under layers of silicon wafers with high precision
- Enables high throughput and highly reproducible inspection, even for extremely small alignment marks

Applications

- Overlay measurement for Die-to-Wafer stacking processes



OLIC Series Die-to-Wafer Overlay Measurement System

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